Name: AYTHA RAMESHKUMAR

Designation: Associate Professor

Department: Electronics and Communication Engineering

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Experience (inyears):Teaching:20 yrs Research:00 Others (Industry):4yrs

## 1.Educational / Technical qualifications:

| S.No | Level (UG / PG / Ph.D) | Year of passing  | Specialization |
|------|------------------------|------------------|----------------|
| 1    | B.E.                   | 1991             | Electronics    |
| 2    | M. Tech.               | 2006             | VLSI Design    |
| 3    | Ph.D.                  | Thesis Submitted | VLSI Design    |

#### 2. Teaching and Learning:

- 2.1 TeachingInterests:
  - VLSI Design,IOT, Micro controllers and its Applications, Microprocessors, CPLD &FPGA Architectures & Applications, Wireless communication and embeddedsystems.
- 2.2 Novel Teaching & Learning Techniquesadopted: PPTs, Videos, Group Discussions, POGIL, Chalk and Talk, WIT &WILetc.
- 2.3 Involvement in curriculum updating /Design:
  - Academic Committee Member for Dept. of ECE for Curriculum design. VNRlab protocol for Microprocessor& Microcontrollers Lab, Embedded SystemsLab.

### 3. Co-curricular and Extra-Curricular Activities

- 3.1. Interests and Hobbies: Sports, ListeningMusic
- 3.2. CCA/ECA Organized: Convergence-2k17, Convergence-2k16, Convergence-2k15, Scintillaschunz
- 3.3. CCA/ECAparticipated:
  - Project Evaluation committee member for M.Tech (EmbeddedSystems).
  - Department Entrepreneurship cell in-charge.
  - Student IETE Societyin-charge
- 3.4. Counseling and MentoringActivity:
  - Counselor and mentor for B.TechStudents.

Committees involvedin: Departmentlevel:

- Academic CommitteeMember
- Project Evaluation CommitteeMember
- Technical Seminar Evaluation Member Institute Level:
- In-Charge for Telecom forcollege
- Student IETE societyin-charge
- Department Entrepreneurship cellin-charge

#### 4. Conference / Workshop / Seminar / Guest Lectures:

- 4.1 Conducted:16
  - National conference VelaSiEm-2k7 at VNRVJIET in 2007
  - Short term intensive course on Embedded Architecture & Applicationsat
  - VNRVJIET, Hyderabad on 12-14, February2009
  - Workshop on IOTs & Its Applications at VNRVJIET in 2016 on 12-14, February 2016.
  - Member of the Reception, Decoration, Stage Management committee and Hospitality
- Organized 7<sup>th</sup> IEEE International Advance Computing Conference(IACC2017) at VNRVJIET,Hyderabad on 5<sup>th</sup> -07<sup>th</sup> January2017.
  - 4.2 Attended: ICEEOT- 2016, IACC 2017, E&ICT IITG, NITW, NITP, IITB, KU
  - A week FDP on "LaTeX & Technical Report Writing" from 25<sup>th</sup> to 30<sup>th</sup> May 2020.



- A Five Day FDP on "Establishing Research Beyond Horizon" from 26<sup>th</sup> to 30<sup>th</sup> May 2020.
- Webinar on "Relax, Refresh, Rejuvenate" on 30<sup>th</sup> April 2020.
- Webinar on "Latex A Scientific Documenting Tool" on 21st May 2020.
- One week NIT & JNTUH "5G Technologies" by JNTUH, Hyderabad, 18th Dec-24th Dec 2017.
- One week FDP on "Integrated circuit and System Design Using CAD Tools" by VNRVJIET, Hyderabad from 12<sup>th</sup> -17<sup>th</sup> June 2017.
- Two-week ISTE STTP "CMOS Mixed Signal and RF VLSI Design" by IIT Kharagpur at VNRVJIET, Hyderabad,30th January 2017 to 04th February2017.
- IEEE International Conference on Electrical, Electronics and Optimization Techniques, at DMI College of Engineering, Chennai, 3-5<sup>th</sup>, March2016.
- FDP on "Trends in wireless Technologies and Evolution of Simulation tools, at VNRVJIET, 11-23, May2015.
- TEQIP- II sponsored training program on "VLSI Design Flow Using CAD Tools and Hardware Implementation" at VNRVJIET, Hyderabad, 27thJuly-07th August 2015.
- 7th IEEE International Conference on Technology for Education at NIT, Warangal,10-12, December 2015.
- "Three Day Workshop on Outcome Based Accreditation" by NBA Nodal Centre, JNTU Hyderabad, 15th-17th February2014.
- Workshop on ASIC Design Flow Using Industry Standard EDA Tools organized by VNRVJIET on 21st-27th June 2013.
- Workshop on Wireless Sensor Nodes by VNRVJIET on 19 th-20th June2013.
- Seminar on Research Publications and Documentation by VNRVJIET, Hyderabad on 04th May2013.
- Three day International conference on REIMAGINE STEM at VNRVJIET Hyderabad.
- Workshop on "Low Power VLSI Design Methodologies" by SYNOPSYS at CVED JNTUH, Hyderabad, INDIA.
- Work shop on "VLSI Design Methodologies" by SYNOPSYS at Padmasree B.V.Raju Institute of Technology, Narsapur, INDIA, 6th -7th March2009.

#### 5. Academic Contribution and Research & Consultancy:

- 5.1.Invited Lectures:
  - Delivered Guest lecture on overview of Internet of things in VNRVJIET
  - Delivered Guest Lecture on VLSI Design at Lords Institute of Engineering & Technology, Hyderabad –November 2014
  - Delivered Lecture in FDP on Recent trends in Embedded Systems design in VNRVJIET in November2013.
- 5.2. Articles/Chapters published in Books:Nil
- 5.3. Books published as single author or as editor:Nil
- 5.4. ProjectsGuided:

a)UG:20 b)PG:20

5.5. Research Interests: VLSI design, Data Transmission Protocols and

ProcessorArchitectures and

EmbeddedSystems

5.6. Ph.D students:Nil

a)Enrolled:Nil b)Submitted:Nil c) Awarded:Nil

5.7. Papers published in reviewedJournals:

| S.No | Title of the Paper  | ournal Name<br>Vol.No.PP   | ISBN/ISSN<br>No.                         | Impact<br>Factor/<br>Citation<br>Index | National/<br>International |
|------|---|--|--|--|----------------------------|
| 1    | Hierarchical Matched Filter<br>Implementation on FPGA<br>for WCDMA<br>Systems   | Journal of<br>Communication and<br>Computer, USA.August<br>2011,<br>Vol8, PP 686-692.  | ISSN<br>No.1548-<br>7709                 | 2.69                                   | International              |
| 2    | Emotion Recognition from<br>Speech Using Embedded<br>Board OMAP 3530  | IJARET, India, October 2013, vol.1, issue ix, October 2013,38-44PP.  | ISSN 2320-<br>6802                       | 2.375                                  | International              |
| 3    | Implementation of High efficiency High throughput and low power design for high order filter using distributed architecture Implementation of High efficiency High throughput and low power design for high order filter using distributed architecture | International journal for<br>Innovative Engineering<br>and Management<br>Research, vol.6,issue<br>13, December<br>2017,172-180pp |  | 7.8                                    | International              |
| 4    | Implementation of Primary<br>Synchronization signal<br>Detection in LTE   | International journal of<br>Advance Engineering<br>and Research<br>Development, Volume<br>5, Issue 04, April 2018                | ISSN : 2348-<br>6406                     | 5.71                                   | International              |
| 5    | Implementation of Secondary Synchronization in LTE  | IJCRT, 2018  | ISSN: 2320-<br>2882                      | 5.97                                   | International              |
| 6    | Implementation of synchronization for 5G NR system  | Advanced Science<br>Letters, Vol. 26,<br>No. 06, 129-135pp.  | E-ISSN:<br>1936-7317                     | 6.224                                  | International              |
| 7    | Implementation of 5G<br>NR Primary and<br>Secondary<br>Synchronization  | Turkish Journal of<br>Computer and<br>Mathematics<br>Education, Vol.12,<br>No.8, 2021,3153-<br>3161P.P.                          | E-ISSN:<br>1309-4653                     | 0.32                                   | International SCOPUS       |
| 8    | FPGA Implementation of 5G NR Primary and Secondary Synchronization  | & Continua, Tech<br>Science Press,<br>vol.73, no.1,2022,<br>1585-1600pp.   | DOI:<br>10.32604/cm<br>c.2022.02157<br>3 | 3.7                                    | SCI                        |

<sup>5.8.</sup> Papers presented at National / International conferences:

| S.No | Title of the Paper  | f the Conference/ Seminars   | National/<br>International | Period                        |
|------|---|--|----------------------------|-------------------------------|
| 1    | Performance Evaluation For Digital Matched Filters  | National conference on<br>VLSI & Embedded Systems  | National                   | June<br>2009                  |
| 2    | Hybrid Form Hierarchical<br>Matched Filter on Field<br>Programmable Gate Arrays<br>based on WCDMA | International Conference on<br>Systemics, Cybernetics, and<br>Informatics (ICSCI-2010)                                   |                            | January<br>2010.              |
| 3    | Implementation of Hierarchical<br>Matched Filter on FPGA for<br>WCDMA Systems                     | International Conference on<br>Advances in Information,<br>Communication Technology<br>and VLSI Design (ICAICV-<br>2010) |                            | August<br>2010                |
| 4    | 1 1   | IEEE International Conference on Electrical, Electronics and Optimization Techniques,                                    |                            | March<br>2016.                |
| 5    | The Fastest Possible Solution to the Weighted Water – Filling Problems                            | 7 <sup>th</sup> IEEE International<br>Advanced Computing<br>Conference (IACC 2017)                                       |                            | January<br>2017               |
| 6    | Energy Efficient Adiabatic Logic<br>Against Power Analysis Attacks<br>for IOT Applications        | `` '   |                            | 18-19<br>November<br>2021     |
| 7    | FPGA Realization of 5G NR<br>Primary Synchronization Signal<br>Detector using Systolic FIR Filter | on Machine Learning, Image   |                            | 11th-12th<br>December<br>2021 |

5.9. Sponsored research Projects:Nil

5.10 Consultancy Projects: Nil

# 6.Awards / Honors received:

Best paper award in International Conference on Systemics, Cybernetics, and Informatics (ICSCI-2010), Pentagram Research Centre, Hyderabad, January 2010.

7. Motto: Work is Worship & Efficiency is Divine Vision, Work & Efficiency SecureLife